VRB Transition Module (VTM-II)

Features

- Converts serial optical data to 20-bit TTL parallel data
- Four 1.5 Gb/sec(max.) serial optical inputs w/ ST connectors
- Single Width 9U x 120mm VIPA Transition Module
- Conforms to VME64x/VIPA , 9U x 400 Format VITA 1.3, Draft .7
- Monitor & Control provided by one microcontroller per channel to:
- Monitor Optical Power of each channel
- Moitor signal detect of optical device
- Reset individual HP Glink devices
- Inhibit switching of output data buffers
- Extensive use of pi filters, ferrite beads to reduce switching noise
- 14 layer pc board w/ 6-layers ground plane to:
- provide 50-ohm striplines for all high speed signals
- Minimize channel-to-channel cross-talk

Description

The VRB Transition Module (VTM-II) is basically a high speed serial to parallel converter incorporating four 1.5Gbit/s(max) serial optical receiver channels on a single width 9U x 120mm standard module (VITA 1.3, draft .7). This module was specifically designed to provide a replaceable optical front-end for the VME Readout Module (VRB) to ease its real estate burden. The VTM-II user inputs to this module is via front panel optical ST connectors. The input optical data is received and converted to a differential ECL data stream by a Finisar FRM-8510 device. The serial bit stream output of the Finisar device is then converted to 20-bit parallel data word by Hewlett Packards's TTL G-Link chip (part# HMP-1024). Each of the four 20-bit parallel TTL data channels is presented to the P5/P6 VME connector for input to the VRB. Also, the VTM-II has an 8-pinmicrocontroller per channel to provide minimal control and monitoring functions (example: optical receiver power, signal detect and channel reset commands). Extensive use of high speed techniques were incorporated into the pc board (ferrite beads, pi filters and stripline vs typical microstrip lines)

The VRB Transition Module (VTM-II) incorporates four optical channels of Finisar's 1.5-Gbit/s receivers (FRM-8510, see datasheet in appendix 1) and Hewlett Packard's TTL G-Link receiver chip (part# HDMP-1024, see datasheet in appendix 2) on a VIPA Standard rear mounted transition module. This module was designed to ease the real estate burden of the VME Readout Buffer (VRB) and to provide system maintainability on an easily replaceable optical interface card. Approximately 300 of the VTMs will be installed for the SVX project in both the CDF and D0 experiments at Fermilab.

The VTM-II is an enhanced version of the Fermilab designed VTM (see section on history) which implements the TTL G-link (HDMP-1024) from Hewlet Packard. The VTM-II retains the Fermilab's original VTM design implementing the low power data buffers, the power/ground plane layout and the extensive use of ferrite beads (to form pi filters) on the power to each device; all concepts which have been positively demonstrated to reduce error rates. A block diagram of the VTM-II is shown in figure 1.

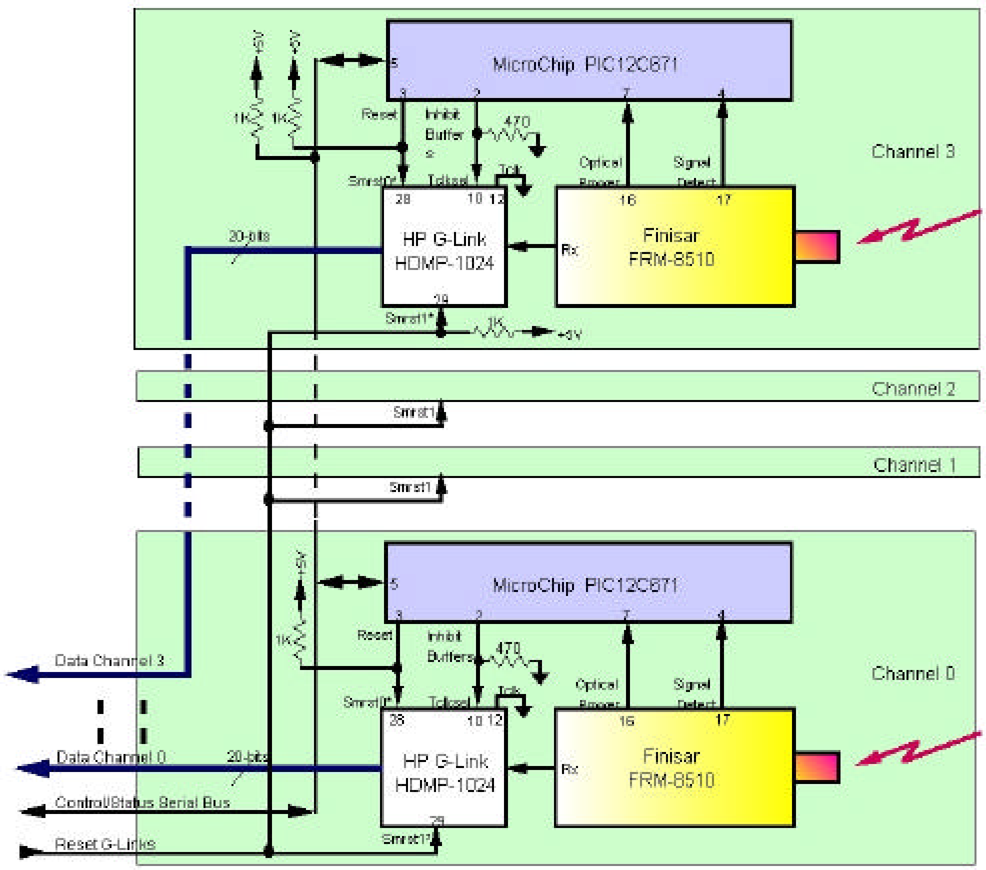


Figure 1. **Block Diagram of VTM-II**

Front Panel Indicators

The VTM has several LEDs on its front panel to indicate the status of the optical input (is the cable plugged in?), +5v power and the jumper options. The LED just below the ST optical connector indicates the input is receiving an optical signal (when LED is on). The LED just above the center front panel mounting screw indicates the +5.0v power is present (LED on). The top two LEDs just below the center mounting screw indicates the status of the pc board frequency selection jumpers as shown in the following table.

DIV1 JP6	DIV0 JP7	DIV1 LED	DIV0 LED	Frequency Range
IN	IN	OFF	OFF	630.0 – 1250 Mhz (default)
IN	OUT	OFF	ON	316.7 – 1067 Mhz
OUT	IN	ON	OFF	158.0 – 533.0 Mhz
OUT	OUT	ON	ON	125.0 – 267.0 Mhz

Table 1.

The third LED down fron the center front panle mounting screw indicates the status of the pc board word selection jumper (JP3). If 20 bit mode is selected the jumper is out (default setting) and the LED is on. For 16 bit mode the the jumper is in and the LED is on.

J3 Connector Pin Assignments

PIN	ROW E	ROW D	ROW C	ROW B	ROW A
1	L2_D0	GND	sc	GND	L0_D0
2	L2_D1	L2_D2	sc	L0_D2	L0_D1
3	GND	L2_D3	sc	L0_D3	GND
4	L2_D5	L2_D4	sc	L0_D4	L0_D5
5	L2_D6	GND	sc	GND	L0_D6
6	L2_D7	L2_D8	sc	L0_D8	L0_D7
7	GND	L2_D9	sc	L0_D9	GND
8	L2_D11	L2_D10	sc	L0_D10	L0_D11
9	L2_D12	GND	sc	GND	L0_D12
10	L2_D13	L2_D14	sc	L0_D14	L0_D13
11	GND	L2_D15	sc	L0_D15	GND
12	L2_D16	L2_D16	sc	L0_D16	L0_D16
13	L2_D17	GND	sc	GND	L0_D17
14	L2_D17	L2_D18	sc	L0_D18	L0_D17
15	GND	L2_D18	sc	L0_D18	GND
16	L2_D19	L2_D19	sc	L0_D19	L0_D19
17	L2_CAV*	GND	sc	GND	L0_CAV*
18	L2_DAV*	L2_LNKRDY*	sc	L0_LNKRDY*	L0_DAV*
19	GND	L2_LNKRDY*	sc	L0_LNKRDY*	GND
20	L2_STRBOUT	GND	sc	GND	L0_STRBOUT
21	L2__Rx_Sig_Det	L2_ERROR	sc	L0_ERROR	L0_Rx_Sig_Det
22	GND	L2_ERROR	sc	L0_ERROR	GND
23	GND	GND	sc	GND	GND
24	GND	GND	sc	GND	GND
25	GND	GND	sc	GND	GND
26	L3_CAV*	GND	sc	GND	L1_CAV*
27	L3_DAV*	L3_LNKRDY*	sc	L1_LNKRDY*	L1_DAV*
28	GND	L3_LNKRDY*	sc	L1_LNKRDY*	GND
29	L3_STRBOUT	GND	sc	GND	L1_STRBOUT
30	L3__Rx_Sig_Det	L3_ERROR	sc	L1_ERROR	L1__Rx_Sig_Det
31	GND	L3_ERROR	sc	L1_ERROR	GND
32	L3_D0	GND	sc	GND	L1_D0
33	L3_D1	L3_D2		L1_D2	L1_D1
34	GND	L3_D3		L1_D3	GND
35	L3_D5	L3_D4		L1_D4	L1_D5
36	L3_D6	GND	GND	GND	L1_D6
37	L3_D7	L3_D8	GND	L1_D8	L1_D7
38	GND	L3_D9	GND	L1_D9	GND
39	L3_D11	L3_D10	GND	L1_D10	L1_D11
40	L3_D12	GND	GND	GND	L1_D12
41	L3_D13	L3_D14		L1_D14	L1_D13
42	GND	L3_D15		L1_D15	GND
43	L3_D16	L3_D16		L1_D16	L1_D16
44	L3_D17	GND		GND	L1_D17
45	L3_D17	L3_D18	*SERIAL*	L1_D18	L1_D17
46	GND	L3_D18	RESET*	L1_D18	GND
47	L3_D19	L3_D19	MODID	L1_D19	L1_D19

Table 2.

VTM Microcontroller

As shown in the diagram, the VTM-II implements four 8-pin microcontrollers (PIC12C671, see datasheet in appendix 3) interconnected to a common control/status serial bus to the VRB (via the VIPA J-3 connector). The following is list of the PIC12C671 benefits:

- Small 8-pin surface mount microcontroller
- 6 - configurable I/O pins
- Four channel ADC
- Sleep mode which inhibits the internal clock oscillator

The PIC12C671 microcontrollers are generally in a listening/sleep mode. Control information is passed to the microcontrollers via an eight bit serial data stream from the VRB and status is passed back on the same line. The serial bit stream consist of the 3-bit channel address and a 5-bit command. The microcontrollers perform the following monitor and control functions per VTM optical channel:

1. Monitor the optical power of each Finisar Receiver (FRM-8510) .
2. Monitor the Finisar “signal detect’ status line.
3. Reset individual HP G-link devices.
4. Disable the clock & data buffers to reduce switching noise on an individual G-link device.
   - Assert one of the G-Link reset lines (SMRST0*). This holds the receiver state machine in state 0; inhibiting the output data buffer from switching. This guarantees the output of the data buffer to be static; however, its state (high or low) will be unknown.
   - To inhibit the clock buffer the output data buffer, assert Tclksel with Tclk connected to ground (logic low). The state of the buffer outputs are static but the level is undefined. Confirmed by Prasad of H.P. Shuting down the power to the device was initially recommended by H.P.
   - Shut down the power to individual sections of the VTM by implementing highside power switches.
5. Report the status of item 1 & 2 to the VRB upon request.

Finisar Optical Power Monitoring

The Finisar transmitter (FTM-8510) and receiver (FRM-8510) were designed to operate as a pair (full duplex mode) with the transmitter having a serial command/status port. As a pair, status of the receiver can also be readout like the transmitter since several of the status signals (including optical power) on the receiver are connected to the transmitter. The transmitter incorporates an 8-bit ADC and a digital serial communicaton port for status read out for both devices. This status information includes transmitter/receiver optical power, calibration numbers, IDs, TX temperature & etc.

When used as a unidirectional device (as in CDF & D0), the receiver optical power monitoring must be either eliminated (as was the case of the first few VTMs &GRTs) or monitored by implementing an external device such as the PIC12C671 8-pin microcontroller. This device is ideal for simple control/status applications where low noise (sleep mode disables oscillator) is its major attribute and speed is its least. The 8-pin microcontroller permits the Finisar analog values (such as the optical power) to be periodically monitored throughout the life of the SVX project.

Adequate optical power (>-13db) guarantees reliable link operation with a minimum Bit-Error-Rate (typically $<10^{-15}$). Monitoring the vital functions of the optical system can help determine when it's time for maintenance and/or device replacement due to optical component aging or infant mortality. Also, during the final system installation at CDF and its testing, the optical attenuation in all FIB-to-VRB links can determined by a simple status request to the VTM-II. This would take all the guess work (& mystery) out of the integrity of the optical transmitters, receivers, cables, connectors and splitters. For a more indepth discussion regarding the usage of Finisar's optical transmitters and receivers see the section "Experience Testing the VTM Prototype".

The Finisar optical receiver (FRM8510) data sheet specificies a Bit Error Rate (BER) of less than 10^{-12} for a pseudorandom bit sequence (10^7 -1) with a typical BER of less than 10^{-15} when the optical power is within the range of +2db to -13db. This tranlates to a voltage range on pin 16 (optical power) of the FRM8510 receiver between ˜ 4.52 volts and ˜ 150mv, respectively. This permits the optical power output pin (16) of the Finisar receiver to be connected directly to the PIC12C671 microcontroller since the analog levels are within the range of the internal 8-ADC (does not require scaling).

Protocol of VRB/VTM Serial Bus

VRB control is sent over the same serial line as the response (optical power & other status) from the VTM. The serial bus is terminated to +5v with a 4.7k-ohm resistor. Data transfer rate on this serial bus is approximately 9600 baud with the timing and protocol as shown in figure 2.

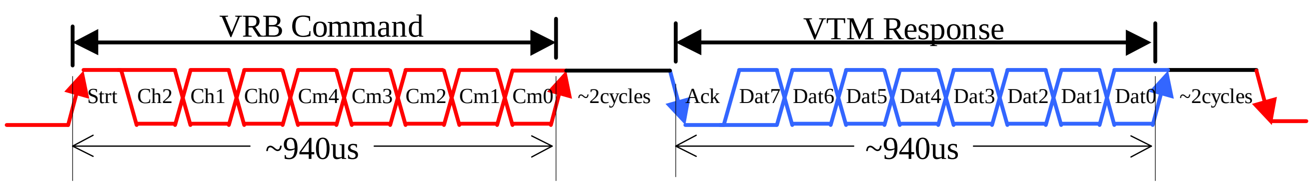


Figure 2.

The signal transitions (figure 2.) initiated by the VRB are shown in red with the blue transitions initiated by the VTM while the black portion represents a tri-stated condition. All transitions with arrowheads are manatory forced levels to indicate the start of a VRB command, the start of a VTM response or a forced level prior to tri-stated condition. The VRB command word consist of a start pulse, a 3-bit channel number, and a 5-bit command. Channel 0 is the optical channel located at the top of the VTM and channel 3 is at the bottom. The most significant bit of the channel number (ch2) is unused in the VTM. Table 3 clarifies the usage of these three bits:

Ch2	Ch1	Ch0	
0	0	0	Optical Channel 0
0	0	1	Optical Channel 1
0	1	0	Optical Channel 2
0	1	1	Optical Channel 3

Table 3.

The VTM accepts only one command per VRB command word sent. The least significant bit of the command word is treated as the highest priority. Therefore, if all bits of the command word are set to a logic one, then Cmd0 (read optical power) will by performed by the VTM. The serial bus must be idle for a minimum duration of 20-bit cycles before sending the next command. The five command bits are defined in table 4.

Cmd4	Cmd3	Cmd2	Cmd1	Cmd0	Command
0	0	0	0	1	Read Optical Power
0	0	0	1	0	Optical Cable Connected
0	0	1	0	0	Disable Channel
0	1	0	0	0	Enable Channel
1	0	0	0	0	Reset Channel

Table 4.

The **Read Optical Power** command (Cmd0) initiates an 8-bit A/D conversion of the analog optical power output of the Finisar FRM-8510 receiver. This 8-bit ADC value is returned in the VTM response following the Cmd0 command. To minimize system bit-error-rates, an ADC value greater than 0x09 (~ -10db) should be maintained. When the value approaches 0x09, its cause should be investigated and corrected. Typical values returned for a FIB connected to a VTM via a 2:1 splitter and two 3’ optical cables with four ST connectors is approximately 0xXX.

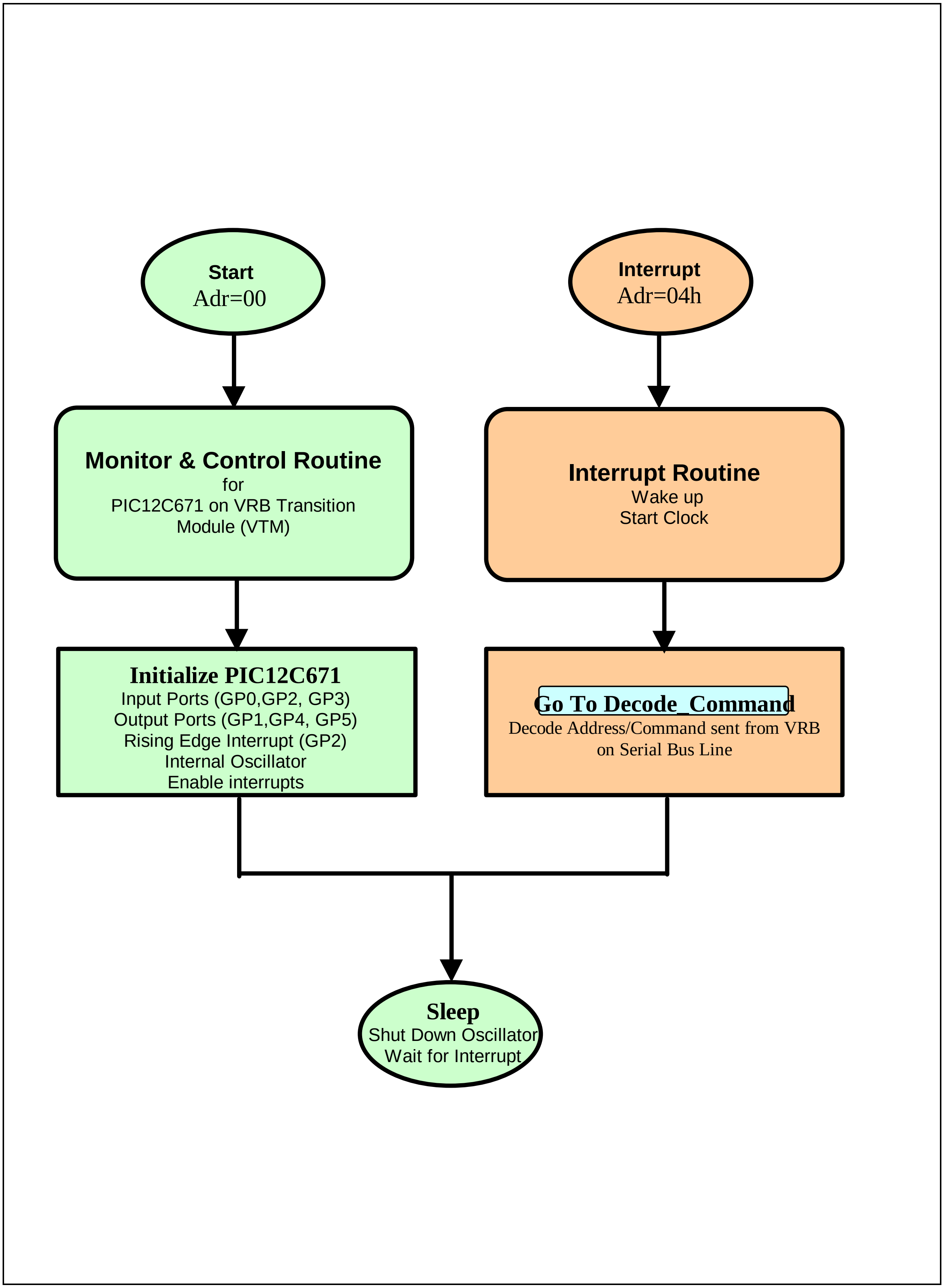
The **Optical Cable Connected** cammand (Cmd1) returns a VTM Response of 0x01 if the optical cable to that channel is connected; otherwise, the value returned is 0x00.

The **Disable Channel** command (Cmd2) inhibits the clock of the HP G-Link which effectively turns off the channel. The VTM response returned is b’1110 1101’.

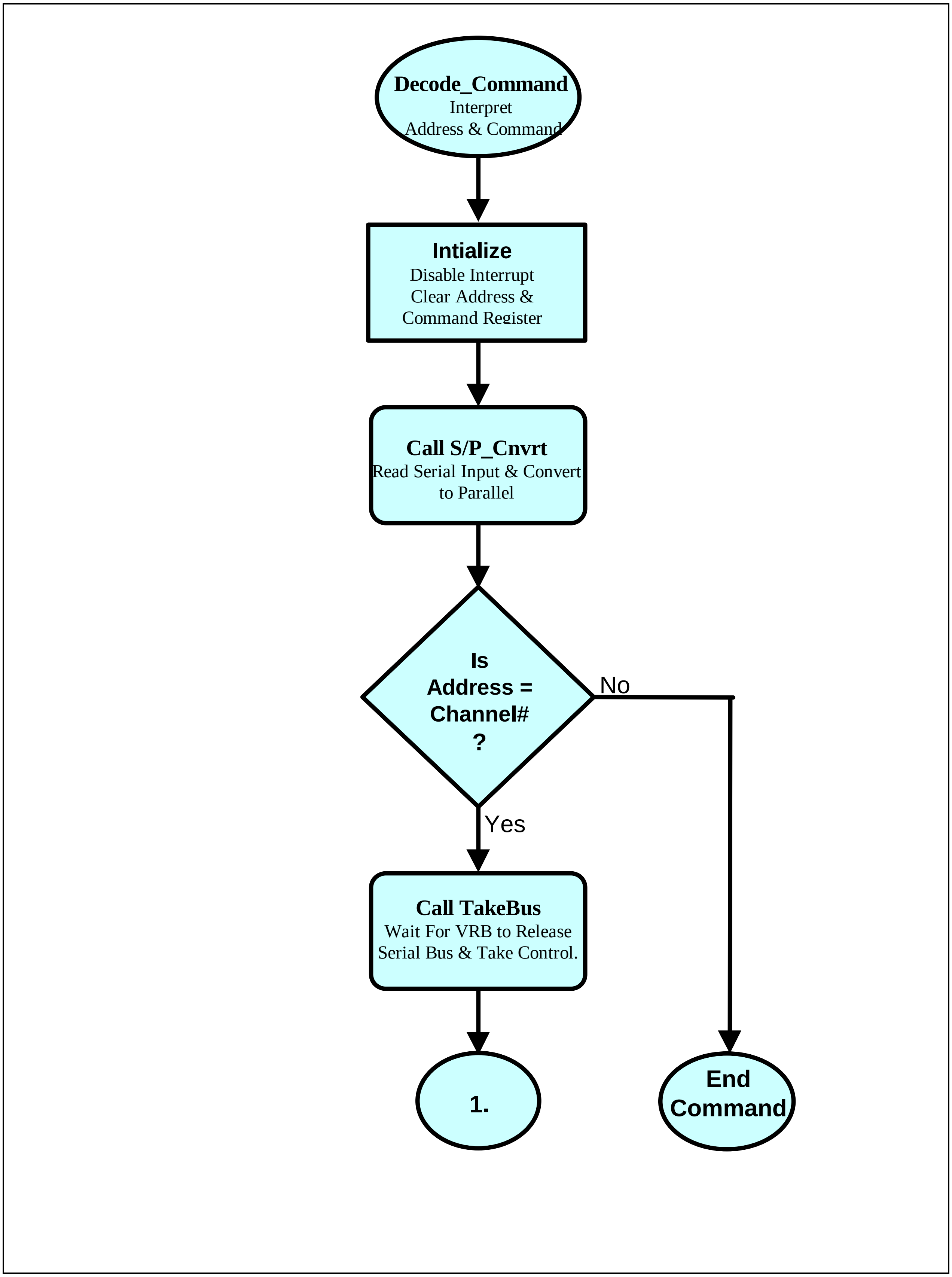
The **Enable Channel** command (Cmd3) enables the G-Link clock and returns the value b’1110 1101’.

The **Reset Channel** command (Cmd4) resets the state machine of the HP G-link device to state zero similar to the global VTM reset line from the VRB except it is on a per channel rather than a per module basis. Again, the value returned is b’1110 1101’.

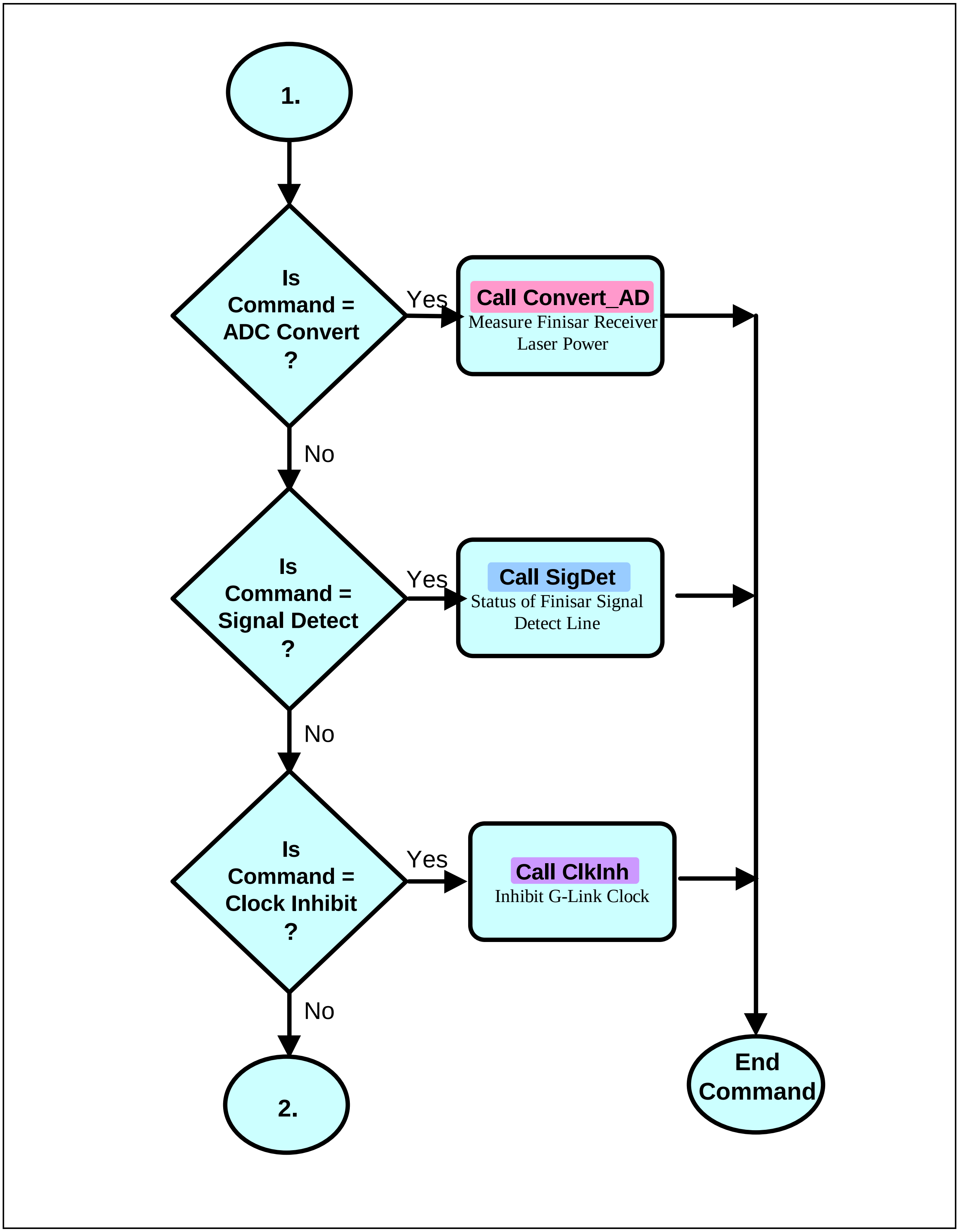
Flow Chart of VTM Microcontroller Program



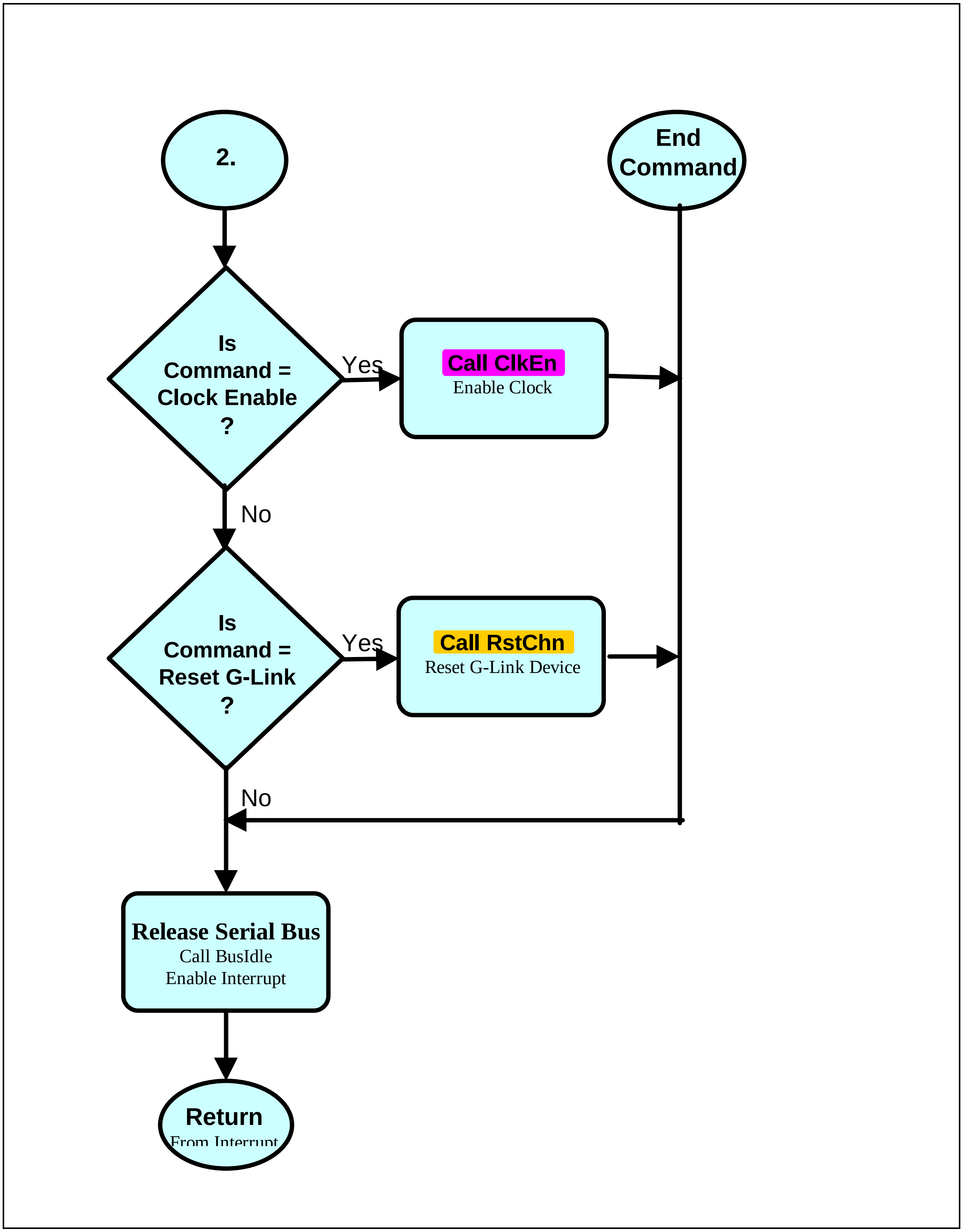
Flow Chart of VTM Microcontroller Program



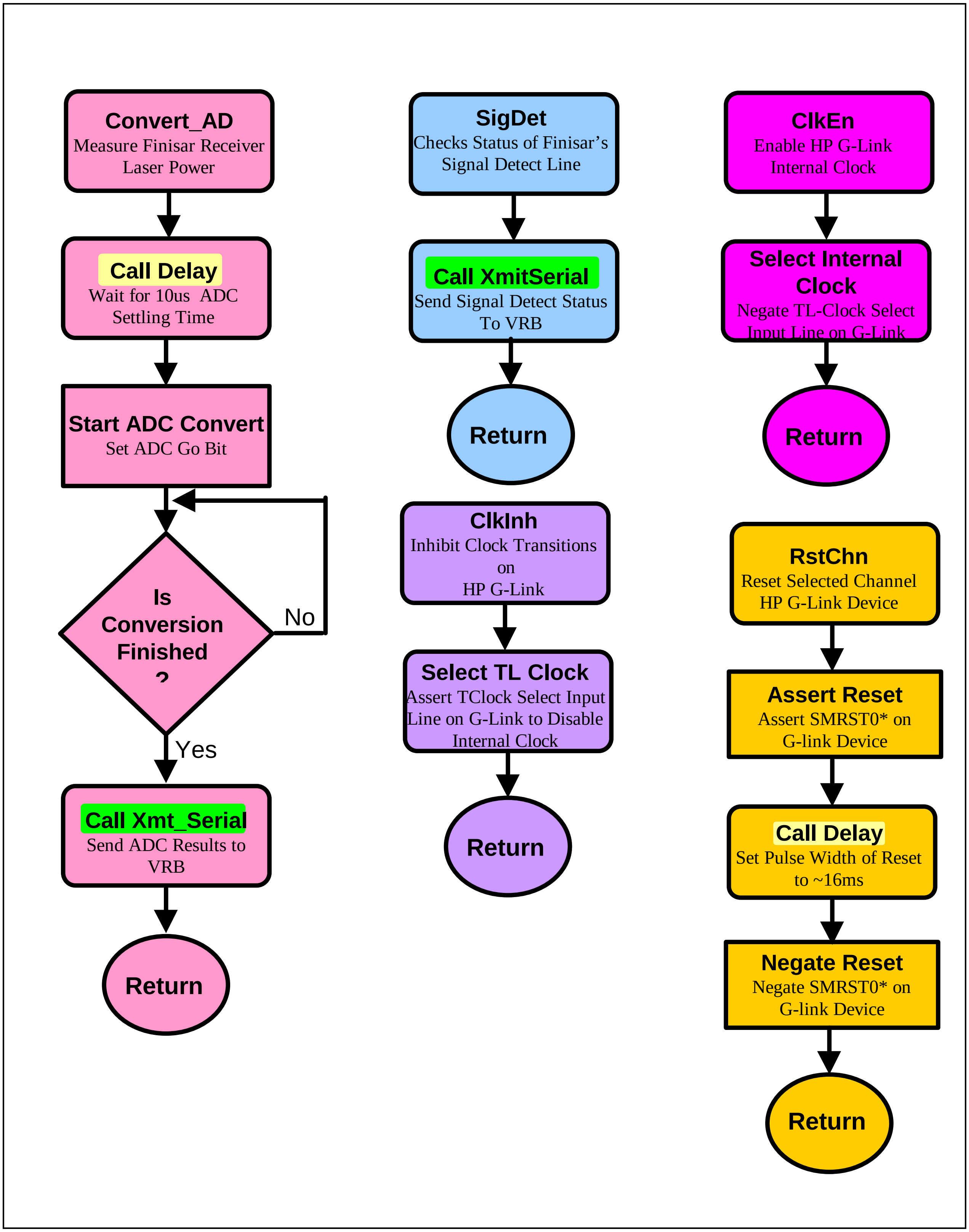
Flow Chart of VTM Microcontroller Program



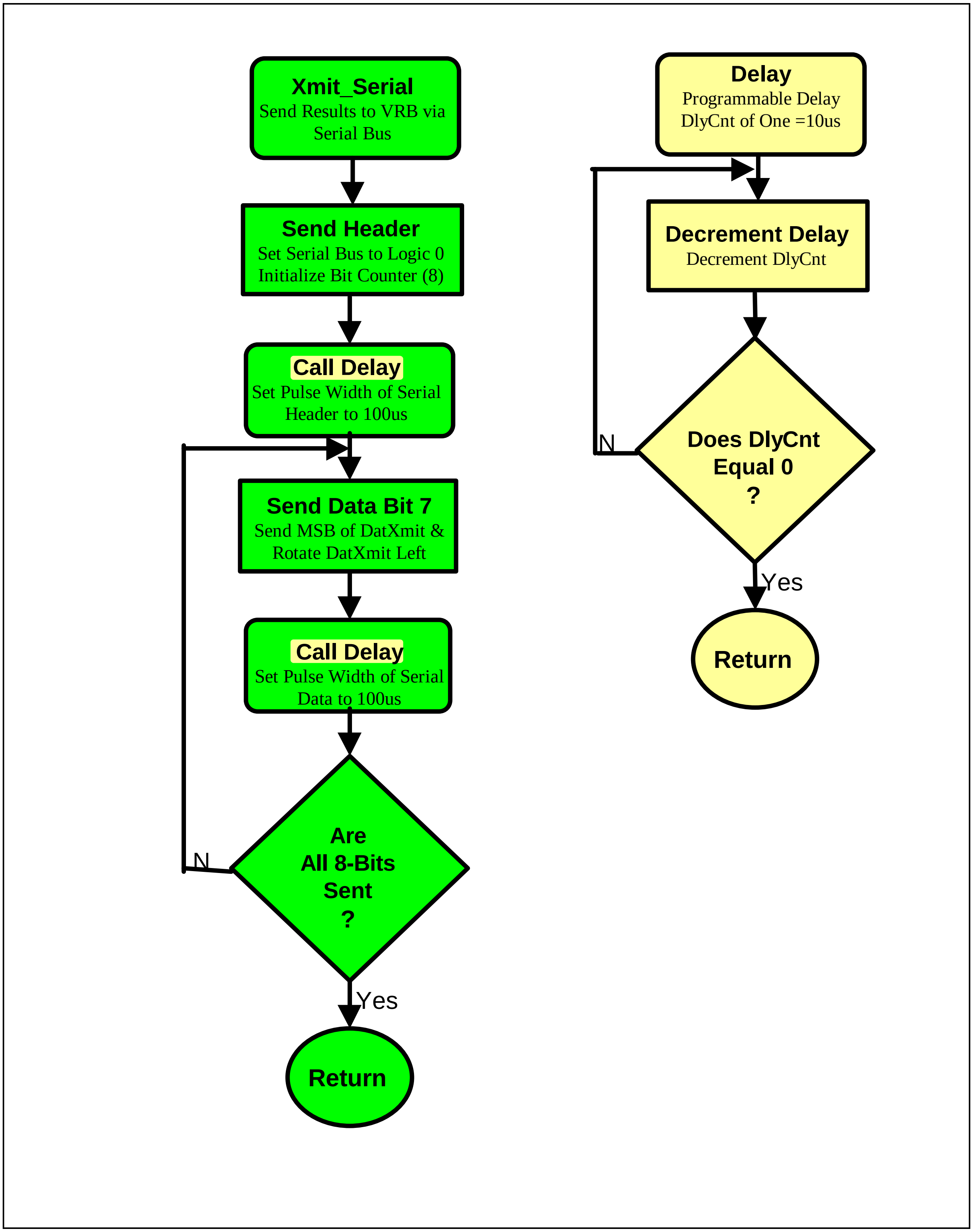
Flow Chart of VTM Microcontroller Program



Flow Chart of VTM Microcontroller Program



Flow Chart of VTM Microcontroller Program



Assembly Program Listing of VTM Microcontroller

```
;TITLE "VTM Optical Power Monitoring & G-link Control     1/29/99"
;This program is performs the following for the Finisar(FRM 8510) @ the HP (HDMP-1024)
;      1. A/D conversion of the optical power of the Finisar device
;            (connected to pin 7 (AN0) of the 12C671)
;      2. Signal detect of the Finisar device
;            (connected to pin 4 <GP3> of the 12C671)
;      3. TCLKSEL to the HP (HDMP-1024) device
;            (connected to pin 2 <GP5> of the 12C671)
;      4. SMRST0* to the HP (HDMP-1024) device
;            (connected to pin 3 <GP4> of the 12C671)
;      5. Single wire serial bus from the VRB
;            (connected to pin 5 <INT> of the 12C671)
;      6. Individual Channel Highside Power Switch (not implemented)
;            (connected to pin 6 <GP1> of the 12C671)
;
;The A/D is configured as follows:
;      Vref = +5V internal.
;      A/D Osc. = internal RC
;      A/D Channel = CN0
;
      LIST P=12C671
      ERRORLEVEL -302
;
      include "p12c671.inc"
      LIST
;P12C671.INC Standard Header File, Version 1.00 Microchip Technology
      LIST
;
;PIC Chip Register bits
GP0   equ H'00'
GP1   equ H'01'
GP2   equ H'02'
GP3   equ H'03'
GP4   equ H'04'
GP5   equ H'05'
;
;
;Delay Variables
Dly1  equ 0x20           ;Inner loop of SMRST* Delay (20)
dly1  set .20
Dly2  equ 0x21           ;Outer loop of SMRST* Delay (255)
;
;
;Variables and constants for converting the serial bit stream from the VRB
;into an 8-bit word containing the channel# and the VTM command for that
;channel #.
HdDly  equ .14                ;One half the pulse width of the Serial data to
;                        strip off the header.
;                        PulseWidth = (HdDly * 3 + 5)microseconds.
DatDly equ .30                ;Pulse width of the Serial data from VRB.
;                        period = (DatDly * 3 + 8)microseconds for the
;                        internal 4Mhz clock with a 1usec instruction rate.
;                        This is approximately 9600 baud.
;Variables
DlyCnt equ 0x22               ;Loop counter for serial bit stream
AdrCmd equ 0x23               ;Contains the combined channe# & command from the VRb
BitCnt equ 0x24               ;Bit Count of the bit stream received from the VRB
DatXmt equ 0x25               ;Variable for transmitting serial data to VRB
Channel     equ 0x26               ;Contains the Channel # received from the VRB
Command equ 0x27              ;Contains the command received from the VRB
;Constants
Ch_Id  equ 0             ;Channnel ID=(0-3) for this PIC chip and must be
;                        programmed for the particular channel # of the VTM
;
```

```
;
	ORG 0x00
	goto Init
;
	org 0x04
	goto Decode_Command	;Interrupt vector to intrepete serial command.
	sleep		;
;
;
	org 0x10
Init
	call Init_PicChip
Start
	sleep
	goto Start
;
; First UV eraseable devices has following instruction at 0x3ff:
;03FF  3490		retlw  0x90 sn#1
;03FF  348C		retlw  0x8C	sn#2
;03FF  348C		retlw  0x8C	sn#3
;03FF  3484		retlw  0x84	sn#4
;03FF  349C		retlw  0x9C	sn#5
;03FF  3494		retlw  0x94	sn#6
;03FF  3490		retlw  0x90	SN#7
;
Init_PicChip
	bsf STATUS, RP0		;Switch to bank1.
	clrf INTCON		;Clear all interrupt enable and flag bits.
	clrf PIE1		;Disable A/D interrupt.
	call 0x03FF		;Get the oscillator calibration number from last program memory
location.
	movwf OSCCAL		;Move calibration number to OSCCAL register. Oscillator now
calbibrated.
	movlw B'00001101'	;Sets GP0,GP2 & GP3 to inputs and GP1, GP4 &
	movwf TRISIO		; GP5 as outputs (GP3 is an input only)
	movlw B'00000110'	;Set GP0 to analog input w/ Vdd as reference
	movwf ADCON1			; and GP1,GP2,GP3,GP4,GP5 as digital.
	bsf OPTION_REG,INTEDG	;Set GP2 as rising edge interrupt.
	bcf STATUS, RP0		;Return to bank0.
	movlw B'11000001'	;Selects ch0, internal RC oscillator and
	movwf ADCON0			; A/D operating mode.
	clrf ADRES		;clr A/D result register
	bsf GPIO,GP4		;Set Glink signal SMRST0* to logic high (GP4)
	bcf GPIO,GP5		;Set Glink signal TClkSel to logic low (GP5)
	movlw B'10010000'	;Set global and interrupt enable & Flag bits.
	movwf INTCON
	return
;
;
;This interrupt routine interprets the channel # and the command that is read by
; the serial conversion routine (Ser_Conv)
;
Decode_Command			;Interrupt routine which interprets the serial input
;			  data stream from the VRB.
	bcf INTCON,INTE		;Disable interrupt on GP2.
	movlw 0			;Load working register w/ 0
	movwf AdrCmd		;Clear address/command register
	bcf STATUS,C		;Clear carry bit of status register
	call SerConv		;Call routine to read convert serial data.
	movf Channel,0			;Compare Channel # received from VRB w/
	sublw Ch_Id		; VTM's Ch_Id. If equal then respond to
	btfss STATUS,Z			; the command, else this channel is not
	goto CmdEnd		; selected, clear interrupts and return.
	Call TakeBus		;Assert logic one on GP2 to take control
;			  of the serial bus.
Commands
	btfsc Command,0		;Check zero'th bit of Command
```

```
      call Convert_AD           ;Measure the optical power of Finisar device
      btfsc Command,0     ;Again, Check zero'th bit of Command and skip
      goto CmdEnd         ; remaining command checks if set.
      btfsc Command,1           ;Check first bit of Command
      call SigDet         ;Check and send status of signal detect line.
      btfsc Command,1     ;Again, Check first bit of Command and skip
      goto CmdEnd         ; remaining command checks if set.
      btfsc Command,2           ;Check second bit of Command
      call ClkInh         ;Inhibit G-link clock by switching to TL_Clock
      btfsc Command,2     ;Again, Check second bit of Command and skip
      goto CmdEnd         ; remaining command checks if set.
      btfsc Command,3           ;Check third bit of Command
      call ClkEn          ;Enable G-link internal clock
      btfsc Command,3     ;Again, Check third bit of Command and skip
      goto CmdEnd         ; remaining command checks if set.
      btfsc Command,4           ;Check fourth bit of Command
      call RstChn         ;Reset HP G-link device
      goto CmdEnd         ;Skip Bus Idle phase.
CmdEnd
;     bsf GPIO,GP2        ;Set SerialBus to a logic one before releasing bus
      bsf STATUS,RP0            ;Switch to bank 1
      bsf TRISIO,GP2            ;Tri-state GP2
      bcf STATUS,RP0            ;Switch back to bank 0
      Call BusIdle        ;Wait for serial bus to become idle
      bcf INTCON,INTF           ;Clear GP2 interrupt flag
      bsf INTCON,INTE           ;Enable GP2 interrupt
RetSleep
      retfie              ;Return from interrupt
;
;
;This routine reads the serial data on the GP2 pin at a 64usec per bit rate
;and converts the stream to an eight bit data word into the variable AdrCmd.
;The format of the variable AdrCmd is as follows:
;-----------------
;|7|6|5|4|3|2|1|0|
;|- - -|- - - - -|
;|-Ch#-|-Command-|
;-----------------
;This variable is then seperated into the two variables Cannel and Command.
SerConv                   ;
      movlw 8                   ;Set bit count loop index to 8
      movwf BitCnt
      movlw HdDly         ;Set bit delay to strip off
      movwf DlyCnt        ; the header bit
      Call Delay
      nop                 ;Kill time to align first bit to 100us boundary
StripBits
      movlw DatDly        ;Set data bit delay to strip bits
      movwf DlyCnt        ; from the data stream on GP2
      Call Delay
      btfsc GPIO,GP2            ;Bit test GP2 input; if zero, skip next instr
      bsf STATUS,C        ; Set carry bit of status register
      rlf AdrCmd,1        ; Rotate AdrCmd left by one bit through carry.
      decfsz BitCnt,1           ;Decrement BitCnt loop; if zero, skip next instr
      goto StripBits            ;Loop back to get next bit.
      movf AdrCmd,0             ;Move contents of AdrCmd to the working register
      andlw B'11100000'   ; strip off the command portion of the byte
      movwf Channel             ; move the contents of the working register to
      swapf Channel,1           ; variable Channel and right justify the channel
      rrf Channel,1             ; number in the variable
      movf AdrCmd,0             ;Move again contents of AdrCmd to the working
      andlw B'00011111'   ; register and mask off the channel portion of
      movwf Command             ; the byte and move the contents to Command
      return
;
;
;
```

```
;The Microchip device that matched the channel# with its ID#, waits for two data
; cycles before sending a start header to the VRB by assertig a logic
; zero on the serial data bus.
TakeBus
      bsf GPIO, GP2             ;Set Serial Bus to a logic one
      bsf STATUS,RP0            ;Switch to bank 1
      bcf TRISIO,GP2            ;Set GP2 output enable
      bcf STATUS,RP0            ;Switch back to Bank 0
      movlw DatDly        ;Wait data bit delay
      movwf DlyCnt        ; from the data stream on GP2
      Call Delay
      movlw DatDly        ;Set data bit delay to strip bits
      movwf DlyCnt        ; from the data stream on GP2
      Call Delay
      return              ; of the serial bus.
;
;
;This routine waits for the serial bus to become idle before re-enabling
; interrupts. The serial bus idle is defined as 10 consecutive logic low
; levels on the bus. This avoids the problem with several PIC chips responding
; to the response of the correct PIC chip sending data to the VRB.
BusIdle
      movlw .10           ;Set bit count to 10
      movwf BitCnt
CntIdle
      movlw DatDly        ;Wait data bit delay
      movwf DlyCnt
      Call Delay
      btfsc GPIO,GP2            ;Test serial bus for a logic low
      goto BusIdle        ; If low then decrement BitCnt and
      decfsz BitCnt,1           ; test for 10 consecutive logic low
      goto CntIdle        ; level; if 10 lows then return otherwise
      return              ; go back and try again.
;
;
;
;This routine performs an A/D conversion of Finisar's Receiver Optical
;power output on the VTM transistion module.
Convert_AD                ;Performs an A/D conversion of the optical power
      movlw 3                   ;Software delay of 10uS for the a/d setup.
      movwf DlyCnt        ; At 4Mhz clock, the loop takes 3uS, w/ Delay
      call Delay          ; set at 3 gives about 9us plus the move, etc.
;                           results in a total of >10us
      bsf ADCON0, GO            ;Start ADC conversion
TstDone
      btfsc ADCON0, NOT_DONE    ;Is A/D conversion complete?
      goto TstDone        ;No, go back and check again
      movf ADRES,W              ;Yes, get a/d value
      movwf DatXmt        ;Store the ADC result in variable DatXmt
      call Xmt_Serial           ;Transmit ADC result to the VRB.
      return
;
;
;
;This routine reads the signal detect level from the Finisar optical receiver
;and store the logic level into variable Sig_Det.
SigDet
      clrf DatXmt         ;Clear variable before checking input pin
      bsf DatXmt,0        ;Finisar signal detect is active low (then set bit)
      btfsc GPIO,GP3            ;Test signal detect input pin. If set then
      bcf DatXmt,0        ; clear Sig_Det bit0
      call Xmt_Serial           ;Transmit the siganl detect status to VRB
      return              ;return
;
;
;
```

```
;This routine selects the TCLKSEL of the HP G-link device by setting a logic one
;the GP5 output pin.
ClkInh
      bsf GPIO,GP5        ;Set GP5 to a logic one disabling internal
      movlw 0xED          ;Send something "ED" to VRB as a handshake
      movwf DatXmt        ;
      call Xmt_Serial           ;   Now send it
      return              ; clock of G-Link (selects T-clock)
;
ClkEn
      bcf GPIO,GP5        ;Clears GP5 to a logic zero which enables
      movlw 0xED          ;Send something "ED" to VRB as a handshake
      movwf DatXmt        ;
      call Xmt_Serial           ;   Now send it
      return              ; the internal clock of the HP G-link
;
;
;
;This routine performs a single-channel HP G-link reset by pulsing the SMRST0*
; connected to GP4 to a logic low for approximately 10us.
RstChn
      movlw 0xED          ;Send something "ED" to VRB as a handshake
      movwf DatXmt        ;
      call Xmt_Serial           ;   Now send it
      bcf GPIO,GP4        ;Set GP4 (SMRST0*) to a logic low.
      movlw 20            ;Start pulse width of approximately 16millisec
      movwf Dly1          ; by setting outer loop of pulse width to 20 and
SrtPls
      movlw .255          ; Set outer loop of pulse width to 255 (766us)
      movwf DlyCnt        ; giving approx. 16ms
      call Delay
      decfsz Dly1,1             ; skip next instr if zero.
      goto SrtPls         ;
      bsf GPIO,GP4        ;End Pulse by Setting GP4 (SMRST0*) to a logic high.
      return
;
;
;
;This routine is a software delay of XuS for the a/d setup.
;At 4Mhz clock, the loop takes 3uS,initializing DlyCnt with
;a value of 3 gives 9uS, plus the move & etc  results in
;a total time of > 10uS.
Delay
      decfsz DlyCnt,1
      goto Delay
      return
;
;
;
;This routine transmits an eight bit word w/ a start bit on the GP2 serial port.
Xmt_Serial                ;
      movlw 8                   ;Set bit count loop index to 7
      movwf BitCnt
      movlw DatDly        ;Set bit delay to send the header bit
      movwf DlyCnt
      bcf GPIO,GP2        ;Send header (logic low for VTM header)
      Call Delay          ;Header pulse width delay
      nop
SendBits
      movlw DatDly        ;Set bit delay for the eight bit data stream.
      movwf DlyCnt        ;
      btfsc DatXmt,7            ;If data bit(BitCnt) in variable DatXmt = 1
      bsf GPIO,GP2        ; then set GP2 serial port to a logic one.
      btfss DatXmt,7            ;If data bit(BitCnt) in variable DatXmt = 0
      bcf GPIO,GP2        ; then set GP2 serial port to a logic zero.
      rlf DatXmt,1        ; Rotate DatXmt left by one bit
      Call Delay          ;Pulse width delay for dat stream
```

```
        decfsz BitCnt,1             ;Decrement BitCnt loop; if zero, skip next instr
        goto SendBits               ;Loop back to send next bit.
        bsf GPIO,GP2         ;Force the serial bus to a logic one before
        return               ; releasing the bus.
;
;       org 0x3FF
;       retlw  0x90
        END
```

Experience Testing the VTM Prototype

The prototype VTMs (items 2 & 3 listed above) had significant design changes over the original GRT regarding the power/ground planes, signal routing, power filtering and low power signal buffering. The power/ground planes were designed to isolate the sensitive low level optical circuitry from the potentially noisey TTL circuitry within a particular channel as well as channel-to-channel isolation. Induced noise on the power planes were isolated by implementing Pi filters with ferrite beads on each section of each channel. Also, the power to G-Link device was divided into to three sections (+5v highspeed, +5v core & +5v driver) with seperate pi filters. The buffered signals to the VIPA J-3 connector from each optical channel was routed in individual sections (not intermixed) and isolated between ground planes (strip line) with a 56-ohm characteristic impedance. The back terminating series resistors on the output of the data buffers were not installed (jumpered across) since the low current buffer limits the current into the microstrip data line. The low current buffers (4ma) were chosen to drive the 20-bit parallel data to the VRB via the J-3 connector rather than highspeed high current buffers to minimize noise induced into the power and ground planes. All of these changes were implemented to reduce noise and cross-talk; and inturn, reduce the bit error rate of the device. Some of these changes may have been an overkill but the results from the initial tests of all channels show a drastic improvement over the original GRT.

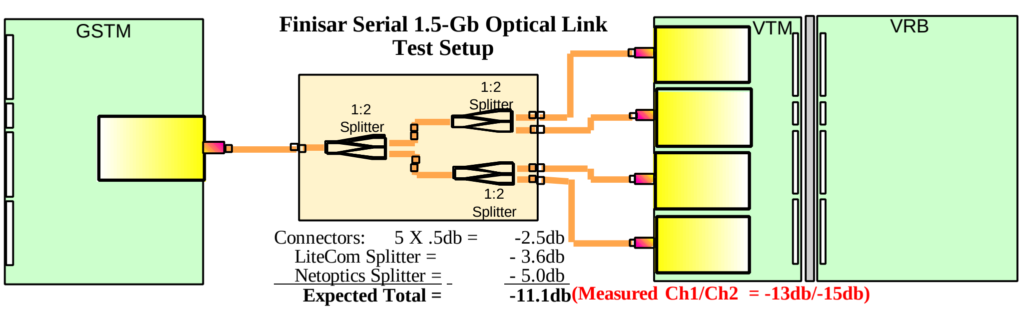


Figure 3

Figure 3 shows a block diagram of the VTM test setup which has one optical channel of a General System Test Module (GSTM) split into four channels at input of the VTM via a two levels of optical splitters (1 x 2 split each). This permits identical data to be sent to all four channels of the VRB to verify whether errors are occurring at the transmitter (same error on all channels) or the receiver (errors only on one channel). The splitters also increases the data rate by a factor of four; thereby, decreasing the test time to acquire a resonable error rate. Based on a rough calculation of the optical power (shown in figure 2), the attenuation was within the limits of the Finisar receiver specification (<13db).

After assembly of several VTM prototypes, preliminary tests indicated a frustratingly low level of errors were occurring on each of the assembled modules. Some of the modules appeared (but only appeared) have a lower error rate than others. During this trouble shooting phase of the VTM it became clear that long term testing (and patience) was necessary to acquire a statistical error baseline. Several ideas were attempted (without success) but the bit error rate of about 8.7 X 10^{-12} plague the VTM project. This resulted in about 3.5 errors per day on four Finisar optical channel based approximately 50-Gbytes of data transferred per day. Once a long term baseline error rate was accumulated several suspected problems were ruled out and an understanding of the VTM problem begin to surface; the loss optical power at the input to Finisar receiver.

The rough calculation of optical attenuation in the system fooled everyone to believe that there was adequate optical power and it could not be a factor in the bit error rate of the VTM test system. An oscilloscope connected to pin 16 of the Finisar receiver device (FRM-8510) was used to measure the received optical power and proved otherwise.

Channel 1		
Attenuator Setting	Actual Attenuation	Optical Power (pin 16)
0db	-3db	1.43V
-5db	-8db	500mv
-7db	-10db	350mv
-10db	-13db	148mv
-12db	-15db	98mv
Channel 2		
Attenuator Setting	Actual Attenuation	Optical Power (pin 16)
0db	-3db	1.56V
-5db	-8db	570mv
-7db	-10db	294mv
-10db	-13db	152mv
-12db	-15db	98mv
Channel 3		
Attenuator Setting	Actual Attenuation	Optical Power (pin 16)
0db	-3db	1.42V
-5db	-8db	432mv
-7db	-10db	298mv
-10db	-13db	154mv
-12db	-15db	102mv

The measurements of the Finisar receiver were calibrated with an optical attenuator (Photodyne 1950XR) confirmed the optical power was much less than originally expected (as shown in figure 2, measured values). The above chart show the results of three of the four channels on the VTM (sn 5) with the Photodyne optical attenuator between it and the GSTM output:

Once the optical power pin (16) on the Finisar receiver was understood, the optical splitters were also calibrated and reconnected (as shown is figure 2) to the VTM to minimize attenuation among the four channel as shown below:

Channel Number	Optical Power (pin 16)
0	161mv
1	148mv
2	146mv
3	174mv

After careful interconnection an optical attenuation of approximately -13db or better was achieved on all channels of the VTM. Knowing that this marginally (at best) met Finisar's specification, long term test proceeded. Over a period of several weeks (including a software revision to increase the transfer rate to approximately 70 Gbytes per day) the bit-error-rate improved by approximately a factor of ten. The rearrangement of the optical splitters (reduced attenuation) reduced the bit-error-rate to approximately 5.1×10^{-13} or 1 error per 3.5 days.

On November 17, 1997 the split of 1 to 4 optical fibers implementing several two channel splitters were replaced with a single four channel device (AMP # 95013-8)as shown in figure 3. The attenuation of this 1 to 4 splitter was measured with ST connectors to be less

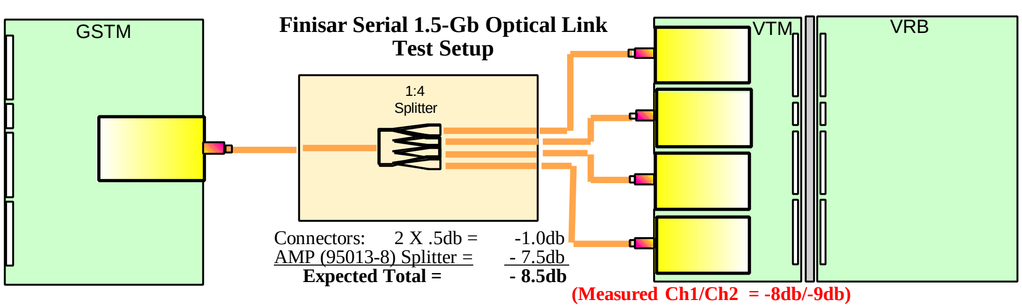


Figure 4

than 8db. Results from a long term test are unknown as of this writing but based on the following measured values of the optical power on pin (16) of the Finisar receivers the bit-error-rate is expected to be significantly lower. The worst case value of 376mv translates to an attenuation less than -8db. However, to verify the effect of greater optical power will require approximately about week of continuous running without errors to accomplish a bit-error-rate of 1×10^{-14} and almost 2 1/2 months for 1×10^{-15}.

Channel Number	Optical Power (pin 16)
0	566mv
1	376mv
2	392mv
3	434mv

Conclusion: the excessive optical attenutation turned out to be the single most important cause of the VTM data errors and its measurement should be incorporated into the next revision.

History of Finisar Optical Transition Module For Data Input to VRB:

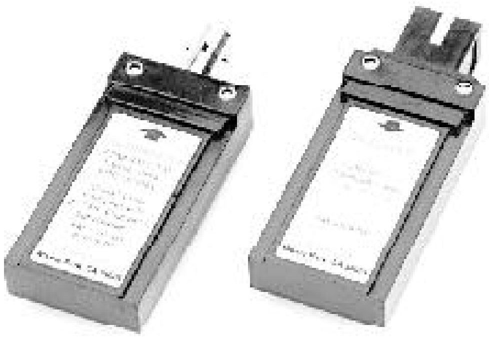
The following recaps the history of the four versions of this module that exist today:

1. The first prototype version was designed at University of Chicago using the ECL G-Link (HP part# HDMP-1014) called a G-Link Readout Transistion Module(GRT). This version was discontinued when HP introduced a TTL version of the G-Link Chip.
2. The second version implemented Finisar’s plugin daughter cards; also containing a ECL G-Link called a VRB Test Module. This was an interim design to be used until the TTL G-Link version was complete.
3. The third version was designed at Fermilab using the TTL G-Link (part# HDMP-1024) called a VRB Transition Module (VTM). Replaced item 1. Cost ˜ $40/channel additional.
4. The fourth version was designed at University of Chicago using the TTL G-Link (part# HDMP-1024). Also replaced item 1. Cost ˜ $40/channel additional.
5. VTM-II (a fifth version) is now under development at Fermilab which incorporates several monitor and control functions. The VTM-II based design is similar to version 3 with the exception of enhancements.

FTM/FRM-8510 **Finisar**

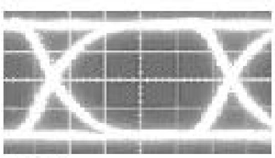
Low Cost, Gigabit

Fiber Optic Transmitter/Receiver

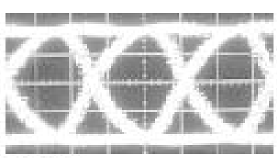


FTM-8510-1 **FRM-8510-2**

These are the 850 nm gigabit transmitter and receiver modules for multi-mode data links of less than 1 Km in length. For long distance links, 1300 nm and 1550 nm single-mode modules are also available in the same package with the same pin-out.



1.0 Gb/s



2.0 Gb/s

Receiver eye patterns from a typical FTM/FRM-8510 link transmitting a 2^7-1 pseudorandom bit sequence.

Also available:

FTR-8510 integrated transceiver module

The FTM-8510 optical transmitter and FRM-8510 optical receiver are two of Finisar's new second generation data link modules. They are excellent building blocks for highly reliable data links at rates up to 1.5 Gb/s. They are designed for LAN applications where data links are usually less than a kilometer in length. For longer distance links, Finisar offers 1300nm and 1550nm single-mode modules with the same package and pin-out. An integrated transceiver module is also available. These second generation Finisar fiber optic links all feature:

- **High speed –** 100 Mb/s to 1.5 Gb/s
- **Low Cost**
- **Very clean and open eye patterns**
- **Very low jitter –** less than 40 ps
- **Low bit error rate –** typically less than 10^{-15}
- **Low power –** < 0.9 Watt total for Tx+Rx
- **Single +5Vdc power supply**
- **Built-in test and diagnostics**
- **Optional ANSI open fiber control built-in**
- **SC or ST optical connectors**
- **Class I laser device**
- **Power saving standby mode**

The FTM-8510 accepts as its data input virtually any differential signal (ECL or PECL) that is > 0.4V P-P. The module is AC coupled and terminated at 50Ω. The data output signal is differential, typically 0.8V P-P.

A unique control and test system is built into all Finisar optical link modules. This system provides real-time control of the optical link as well as status reporting and diagnostics. This control system has a unique interface that enables the user to continuously monitor the status and optical performance of the link. No optical test equipment is required to measure the transmitted and received optical power. The test equipment is built in.

The built-in control/test system has a serial communications port that continuously provides the host system with link status information, optical power levels, drive current, bias voltage, and transmitter temperature. Thus, the host system is able to continually diagnose optical link problems, even while the link is transmitting data. Finisar supplies, at no additional charge, the source code (in ANSI standard C) that enables the user to operate this built-in test and diagnostic system.

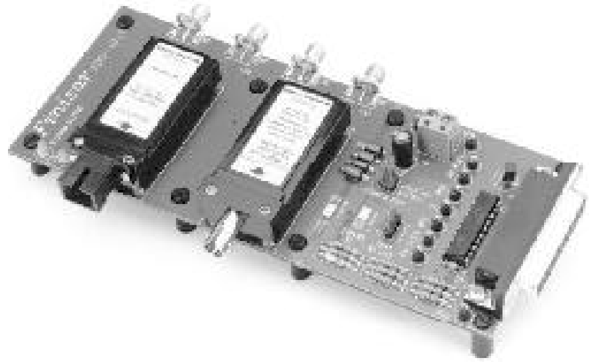
Finisar modules have a low power standby mode that enables the host system to be put in a power conserving standby state. When the receiver receives a light pulse, it signals the host to power up.

Appendix 1

FTM/FRM-8510 Low Cost Gigabit Optical Transmitter/Receiver

Finisar

Pin-out and specifications

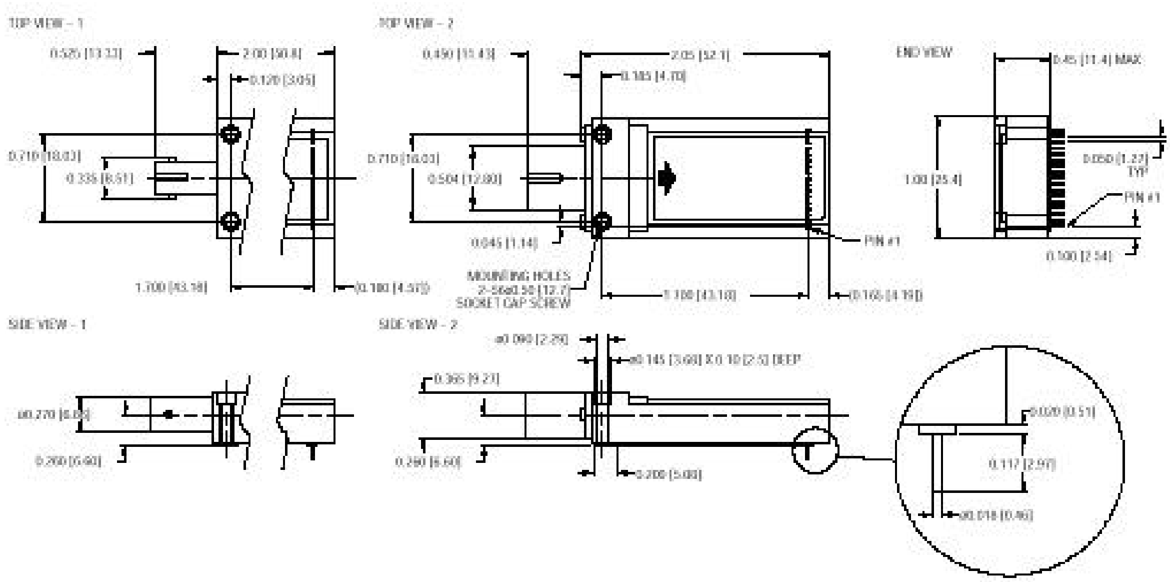


The **FDB-1011 Evaluation Board** is supplied with the transmitter and receiver module mounted in a socket, a software disk, and a DB-25 cable. The board only requires +5Vdc and ground. You supply the differential signal through SMA coax connectors. You may display the output of the built-in test and monitoring system by connecting the FDB-1011 to a PC parallel port.

Part numbers

Transmitter module (850 nm)	FTM-8510-X-Y-Z
Receiver module (850 nm)	FRM-8510-X
Transceiver module (850 nm)	FTR-8510-X-Y-Z
Transceiver evaluation board	FDB-1010-8510-X-Y-Z
Simplex evaluation board	FDB-1011-8510-X-Y-Z

X=optical connector (1=ST, 2=SC), Y=ANSI OFC (1=on, 0=off), Z=data rate for OFC (1=1.06 Gb/s and 531 Mb/s, 2=266 Mb/s)



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Appendix 1

HEWLETT PACKARD

Low Cost Gigabit Rate Transmit/Receive Chip Set with TTL I/Os

Technical Data

HDMP-1022 Transmitter
HDMP-1024 Receiver

Features

- **Virtual Ribbon Cable Replacement**
- **On-Chip Encode / Decode**
- **On-Chip State Machine for Fully Automatic Link Management**
- **On-Chip Tx/Rx PLL Provides Frame Synchronization**
- **High Speed Serial Rate** 150-1500 MBaud (User Selectable)
- **Standard TTL Interface** 16, 17, 20, or 21 Bits Wide
- **Implemented in a Low Cost Aluminum M-Quad 80 Package**

Applications

- **Backplane Serialization/ Bus Extender**
- **Video, Image Acquisition**
- **Point to Point Data Links**
- **Implement SCI-FI Standard**
- **Implement Serial HIPPI Specification**

Description

The HDMP-1022 transmitter and the HDMP-1024 receiver are used to build a high-speed data link for point-to-point communication. The monolithic silicon bipolar transmitter chip and receiver chip are each provided in a standard aluminum M-Quad 80 package.

From the user's viewpoint, these products can be thought of as providing a "virtual ribbon cable" interface for the transmission of data. Parallel data (a frame) loaded into the Tx (transmitter) chip is delivered to the Rx (receiver) chip over a serial channel, which can be either a coaxial copper cable or optical link, and is reconstructed into its original parallel form.

The chip set hides from the user all the complexity of encoding, multiplexing, clock extraction, demultiplexing and decoding. Unlike other links, the phase-locked-loop clock extraction circuit also transparently provides for frame synchronization–the user is not troubled with the periodic insertion of frame synchronization words. In addition, the DC balance of the line code is automatically maintained by the chip set. Thus, the user can transmit arbitrary data without restriction. The Rx chip also includes a state-machine controller (SMC) that provides a startup handshake protocol for the duplex link configuration.

The serial data rate of the Tx/Rx link is selectable in four ranges (see tables on page 5), and extends from 120 Mbits/s up to 1.25 Gbits/s. This translates into an encoded serial rate of 150-1500 MBaud. The parallel data interface is 16 or 20 bit TTL, pin selectable. A flag bit is available and can be used as an extra 17th or 21st bit under the user's control. The flag bit can also be used as an even or odd frame indicator for dual-frame transmission. If not used, the link performs expanded error detection.

The serial link is synchronous, and both frame synchronization and bit synchronization are maintained. When data is not available to send, the link maintains synchronization by transmitting fill frames. Two (training) fill frames are reserved for handshaking during link startup.

User control space is also supported. If Control Available (CAV) is asserted at the Tx chip, the least significant 14 or 18 bits of the data are sent and the Rx Control Available (CAV) line will indicate the data as a Control Word.

Appendix 2

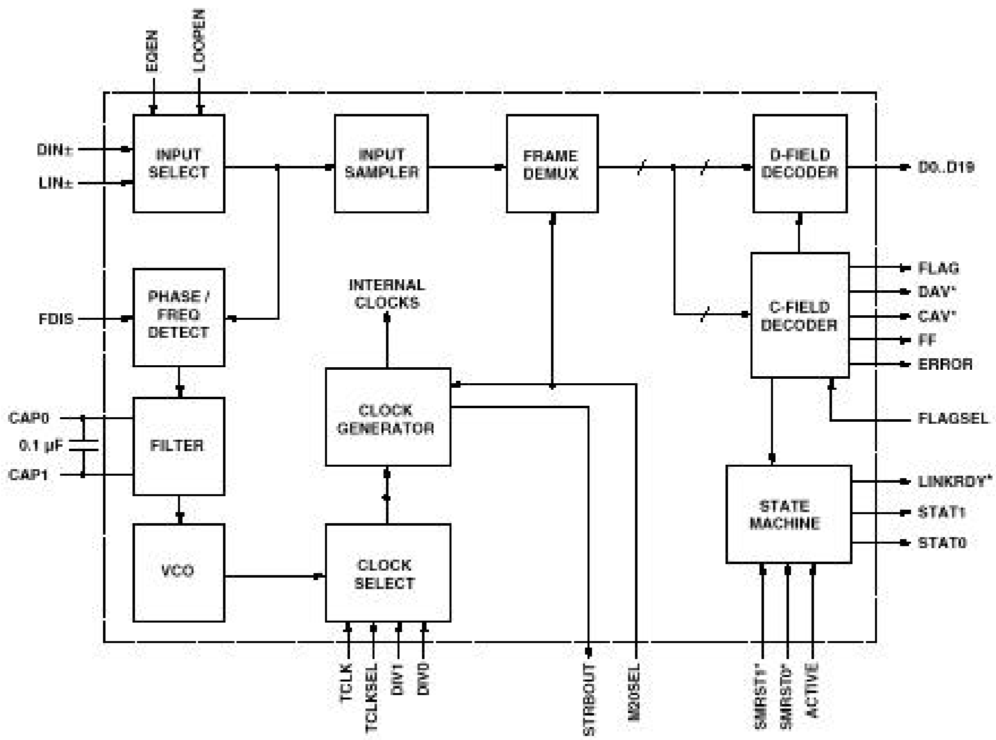


Figure 5. HDMP-1024 Receiver Block Diagram.

HDMP-1024 Rx Block Diagram

The HDMP-1024 receiver was designed to convert a serial data signal sent from the HDMP-1022 into either 16,17, 20, or 21 bit wide parallel data. In doing this, it performs the functions of

- Clock Recovery
- Data Recovery
- Demultiplexing
- Frame Decoding
- Frame Synchronization
- Frame Error Detection
- Link State Control

Input Select

The input select block determines which input line is used. In normal operation (LOOPEN=0), DIN is accepted as the input signal. For improved distance and BER using coax cable, an input equalizer may be used by asserting EQEN. By setting LOOPEN high, the receiver accepts LIN as the input signal. This feature allows for loop back testing exclusive of the transmission medium.

Phase/Frequency Detect

This block compares either the phase or the frequency of the incoming signal to the internal serial clock generated from the Clock Select block. The frequency detect disable pin (FDIS) is set high to disable the frequency detector and enable the phase detector. See *HDMP-1024 (Rx) Phase Locked Loop* for more details. The output of this block, PH1, is used by the filter to determine the control signal for the VCO.

Filter

This is a loop filter that accepts the PH1 output from the Phase/ Frequency Detector and converts it into a control signal for the VCO. This control signal tells the VCO whether to increase or decrease its frequency. The Filter uses the PH1 input to determine a proportional signal and an integral signal. The proportional signal determines whether the VCO should increase or decrease its frequency. The integral signal filters out the high frequency PH1 signal and stores a historical PH1 output level. The two signals combined determine the magnitude of frequency change of the VCO.

VCO

This is the Voltage Controlled Oscillator that is controlled by the output of the Filter. It outputs a high speed digital signal to the Clock Select.

Appendix 2

Clock Select

The Clock Select accepts the high speed digital signal from the VCO and outputs an internal high speed serial clock. The VCO frequency is divided, based on the DIV1/DIV0 inputs, to the input signal's frequency range. The Clock Select output is an internal serial clock. It is phase and frequency locked to the incoming signal. This internal serial clock is used by the Input Sampler to sample the data. It is also used by the Clock Generator to generate the recovered frame rate clock.

By setting TCLKSEL high, the user may input an external serial clock at TCLK. The Clock Select accepts this signal and directly outputs it as the internal serial clock. TCLKSEL is not characterized.

Clock Generator

The Clock Generator accepts the serial clock generated from the Clock Select and generates the frame rate clock, based on the setting of M20SEL. If M20SEL is asserted, the incoming encoded data frame is expected to be 24 bits wide (20 data bits and 4 control bits). In this case the master transition in the control section of encoded data stream is expected every 24 bits, and used to ensure proper frame synchronization of the output frame clock, STRBOUT.

Input Sampler

The serial input signal is converted into a serial bit stream, using the extracted internal serial clock from the Clock Select. This output is sent to the frame demux.

Frame Demux

The Frame Demux demultiplexes the serial bit stream from the Input Sampler into a 20 or 24 bit wide parallel data word, based on the setting of M20SEL. The most significant 4 bits are sent to the C-Field Decoder, while the remaining 16 or 20 bits are sent to the D-Field Decoder.

C-Field Decoder

The C-Field Decoder accepts the control information from the Frame Demux and determines what kind of frame is being received and whether or not it has to be inverted. The control bits are sent to the State Machine for error checking. The decoded information is sent to the D-Field Decoder. CAV* is set low if the incoming frame is control data. When CAV* is low, the state of DAV* is "don't care". DAV* is set low if the information is data. If neither DAV* nor CAV* is set low, then the incoming frame is expected to be a fill frame. If FLAGSEL is asserted, the FLAG bit is restored to its original form. If FLAGSEL is not asserted, FLAG is used to differentiate between the even and odd frames in Double Frame Mode. For more information about this, refer to *Double Frame Mode*.

D-Field Decoder

The D-Field Decoder accepts the data field of the incoming data frame from the Frame Demux. Based on information from the C-Field Decoder, which determines what type of data is being received, the D-Field Decoder restores the parallel data back to its original form.

State Machine

The State Machine is used in full duplex mode to perform the functions of link startup, link maintenance, and error checking. By setting the SMRST0* and SMRST1* low, the user can reset the state machine and initiate link startup. SMRST1* is usually connected to the transmitter's LOCKED output. STAT1 and STAT0 denote the current state of link during startup. ACTIVE is an input normally driven by the STAT1 output. This ACTIVE input is retimed by STRBOUT and presented to the user as LINKRDY*. LINKRDY* is an active low output that indicates when the link is ready to transmit data. Refer to *The State Machine Handshake Protocol* section on page 30 for more details.

Appendix 2

PIC12C67X

8-Pin, 8-Bit CMOS Microcontroller with A/D Converter

Devices Included in this Data Sheet:

PIC12C671 and PIC12C672 are 8-bit microcontrollers with 8-bit A/D Converter packaged in 8-lead packages. They are based on the 14-bit PIC16/17 architecture.

High-Performance RISC CPU:

- Only 35 single word instructions to learn
- All instructions are single cycle (1 μs) except for program branches which are two-cycle
- Operating speed: DC - 10 MHz clock input
  DC - 1 μs instruction cycle

Device	EPROM	RAM
PIC12C671	1024 x 14	128 x 8
PIC12C672	2048 x 14	128 x 8

- 14-bit wide instructions
- 8-bit wide data path
- Interrupt capability
- Special function hardware registers
- Eight-level deep hardware stack
- Direct, indirect and relative addressing modes for data and instructions
- Internal 4 MHz oscillator with programmable calibration
- Selectable clockout
- In-circuit serial programming
- 4-channel 8-bit analog-to-digital converter

Peripheral Features:

- 8-bit real time clock/counter (TMR0) with 8-bit programmable prescaler
- Power-On Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code-protection
- Power saving SLEEP mode
- Interrupt on pin change (GP0, GP1, GP3)
- Internal pull-ups on I/O pins (GP0, GP1, GP3)

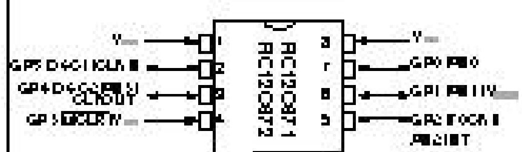
- Selectable oscillator options:
  - INTRC: Precision internal 4 MHz oscillator
  - EXTRC: External low-cost RC oscillator
  - XT: Standard crystal/resonator
  - HS: High speed crystal/resonator
  - LP: Power saving, low frequency crystal
- Internal pull-up on MCLR pin

CMOS Technology:

- Low power, high speed CMOS EPROM technology
- Fully static design
- Wide operating voltage range:
  - Commercial: 2.5V to 5.5V
  - Industrial: 2.5V to 5.5V
  - Extended: 4.5V to 5.5V
- Low power consumption
  - < 2 mA @ 5V, 4 MHz
  - 15 μA typical @ 3V, 32 KHz
  - < 1 μA typical standby current

Pin Diagram

PDIP, SOIC



Appendix 3